SANATAN DHARMA COLLEGE, AMBALA CANTT

College with Potential for Excellence, UGC,New Delhi
NAAC Accredited Grade "A+" with CGPA 3.51 in 3rd cycle
ISO 9001:2015 & ISO 14001:2015 Certified

Department of Computer Science

Lesson Plan (Session 2021-2022)

Class: BCA **SEM: III** **Sec A and Sec B Course Code: BCA-233**
Nomenclature: COMPUTER ARCHITECTURE

Duration: 16 Weeks **Dates: Oct-Jan, 2022**

SYLLABUS

BCA-233 COMPUTER ARCHITECTURE

Maximum Marks: 100 **External: 80** **Minimum Pass Marks: 35**
Internal: 20 **Time: 3 hours**

Note: Examiner will be required to set Nine Questions in all. First Question will be compulsory, consisting of objective type/short-answer type questions covering the entire syllabus. In addition to that eight more questions will be set, two questions from each Unit.Student will be required to attempt FIVE questions in all. Question Number 1 will be compulsory. In addition to compulsory question, student will have to attempt four more questions selecting one question from each Unit.

UNIT -I

Basic Computer Organisation and Design: Instruction Codes, Computer registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory reference instructions, Input-Output and Interrupt, Design of Basic computer, Design of accumulator logic

UNIT -II

Register Transfer and Microoperations: Register Transfer Language (RTL), register transfer, Bus and Memory Transfers, Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift Unit, Microprogrammed Control: Control memory; address sequencing, microprogram sequencer, Design of Control Unit

UNIT -III

Central Processing Unit: General registers Organization, Stack Organization, Instruction formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Program Interrupt, RISC, CISC.

UNIT -IV

Memory Organization: Memory hierarchy, Auxiliary Memory, Associative Memory, Interleaved memory, Cache memory, Virtual Memory, Memory Management Hardware, Input Output Organization : Peripheral devices , Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access(DMA),Input-Output Processor(IOP).

TEXT BOOKS

Computer System Architecture By. Moris Mano, Pearson Education
Computer Architecture and Organization By J.P. Hayes, Tata McGraw Hill

Course Outcomes

After the completion of this course, prospective Computer professionals will have the ability to

CO-1	Understand and explain the basic architecture and design of computer
CO-2	Understand and apply Register Transfer Language (RTL), register transfer, Bus and Memory Transfers
CO-3	Understand and apply Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift Unit
CO-4	Understand and explain Microprogrammed Control
CO-5	Understand and explain Central Processing Unit
CO-6	Understand and explain Memory Organization.

S.No	Instructional Technique	Assessment Methods (AM)
1	Chalk & Talk	**Assignments**
2	ICT tools	**Quiz**
3	Group discussions	**Group Discussions**
4	Industrial visit	**Oral Tests**
5	Case studies	**Sessional**
6	Small Projects	**Presentations**
7	Workshop	**Seminar**
8	Spoken Tutorials	**University Exams**
9	Flipped Class	
10.	**E-Resources**	

Detailed Lesson Plan Sec A

Week	Date	Topic to be Covered	Instructional Technique	Assessment Method
1	11.10.21	**Basic Computer Organisation and Design:**	**2-(PPT/Projector)**	**----**
	12.10.21	**Instruction Codes, Computer registers**	**2-(PPT/Projector)**	**1,2,3,4**
	13.10.21	**Design of accumulator logic**	**2-(PPT/Projector)**	**1,2,3,4**
2	18.10.21	**Computer Instructions**	**2-(PPT/Projector)**	**1,2,3,4**
	19.10.21	Timing and Control	**2-(PPT/Projector)**	**1,2,3,4**
	20.10.21	**Instruction Cycle**	**2-(PPT/Projector)**	**1,2,3,4**
3	25.10.21	Memory reference instructions	**2-(PPT/Projector)**	**1,2,3,4**
	26.10.21	Holiday		
	27.10.21	**Input-Output and Interrupt**	2-(PPT/Projector)	1,2,3,4
4	1.11.21	**RISC, CISC.**	2-(PPT/Projector)	**1,2,3,4**
	2.11.21	**Central Processing Unit:**	2-(PPT/Projector)	1,2,3,4
	3.11.21	**General registers Organization**	2-(PPT/Projector)	1,2,3,4
5	8.11.21	**Stack Organization**	2-(PPT/Projector)	1,2,3,4
	9.11.21	Instruction formats	2-(PPT/Projector)	1,2,3,4
	10.11.21	**Addressing Modes**	2-(PPT/Projector)	1,2,3,4
6	15.11.21	Holiday		
	16.11.21	Program Interrupt	---	6
	17.11.21	**Revision**	2-(PPT/Projector)	1,2,3,4,6
7	22.11.21	**Memory Organization**	2-(PPT/Projector)	1,2,3,4,
	23.11.21	**Memory hierarchy**	2-(PPT/Projector)	1,2,3,4,
	24.11.21	Diwali Vaccation		
8	29.11.21	**Auxiliary Memory**	2-(PPT/Projector)	1,2,3,4
	30.11.21	**Associative Memory**	2-(PPT/Projector)	1,2,3,4
	1.12.21	**Revision**		1,2,3,4
9	6.12.21	**Cache memory**	2-(PPT/Projector)	1,2,3,4
	7.12.21	**Data Transfer and Manipulation, Program Control**	2-(PPT/Projector)	
	8.12.21	**Virtual Memory**	2-(PPT/Projector)	1,2,3,4
10	13.12.21	**Memory Management Hardware**	2-(PPT/Projector)	1,2,3,4
	14.12.21	**Input Output Organization**	2-(PPT/Projector)	1,2,3,4
	15.12.21	**Peripheral devices**	2-(PPT/Projector)	1,2,3,4
11	20.12.21	**Input-Output Interface**	2-(PPT/Projector)	1,2,3,4
	21.12.21	**Asynchronous data transfer**	2-(PPT/Projector)	1,2,3,4
	22.12.21	**Revision**	--	
12	27.12.21	**Modes of Transfer**	2-(PPT/Projector)	1,2,3,4
	28.12.21	**Priority Interrupt**	2-(PPT/Projector)	1,2,3,4

	29.12.21	**Direct Memory Access(DMA)**	2-(PPT/Projector)	1,2,3,4
13	3.1.22	**Input-Output Processor(IOP)**	2-(PPT/Projector)	1,2,3,4
	4.1.22	**Design of Basic computer**	2-(PPT/Projector)	1,2,3,4
	5.1.22	**Register Transfer and Microoperations**	2-(PPT/Projector)	1,2,3,4
14	10.1.22	Register Transfer Language (RTL), register transfer, Bus and Memory Transfers	2-(PPT/Projector)	1,2,3,4
	11.1.22	**Logic Microoperations**	2-(PPT/Projector)	1,2,3,4
	12.1.22	**Arithmetic Microoperations**	2-(PPT/Projector)	1,2,3,4
15	17.1.22	**Shift Microoperations**	2-(PPT/Projector)	1,2,3,4
	18.1.22	**Arithmetic Logic Shift Unit**	2-(PPT/Projector)	1,2,3,4
	19.1.22	**Interleaved memory**	2-(PPT/Projector)	1,2,3,4
16	24.1.22	**MicroprogrammedControl:Control memory**	2-(PPT/Projector)	1,2,3,4
	25.1.22	address sequencing, microprogram sequencer	2-(PPT/Projector)	1,2,3,4
	26.1.22	**Design of Control Unit, Question paper discussion**	2-(PPT/Projector)	--

Detailed Lesson Plan Sec B

Week	Date	Topic to be Covered	Instructional Technique	Assessment Method
1	11.10.21	**Basic Computer Organisation and Design:**	**1**	**----**
	12.10.21	**Instruction Codes, Computer registers**	**1**	**1**
	13.10.21	**Design of accumulator logic**	**1**	**1**
2	18.10.21	**Computer Instructions**	**1**	**1,2,3,4**
	19.10.21	Timing and Control	**1**	**1,2,3,4**
	20.10.21	**Instruction Cycle**	**1**	**1,2,3,4**
3	25.10.21	Memory reference instructions	**2-(PPT/Projector)**	**1,2,3,4**
	26.10.21	**Input-Output and Interrupt**	**2-(PPT/Projector)**	**1,2,3,4**
	27.10.21	**RISC, CISC.**	**2-(PPT/Projector)**	**1,2,3,4**
4	1.11.21	**Holiday**	**--**	**---**
	2.11.21	**Central Processing Unit:**	**2-(PPT/Projector)**	**1,2,3,4**
	3.11.21	**General registers Organization**	**2-(PPT/Projector)**	**1,2,3,4**
5	8.11.21	**Stack Organization**	**9,10**	**1,2,3,4**
	9.11.21	Instruction formats	**9,10**	**1,2,3,4**
	10.11.21	**Addressing Modes**		**1,2,3,4**
6	15.11.21	Program Interrupt	**---**	**6**
	16.11.21	**Memory Organization**	**9**	**1,2,3,4,6**

	17.11.21	**Memory hierarchy**	**6**	**1,2,3,4,**
7	22.11.21	**Auxiliary Memory**	**6**	**1,2,3,4,**
	23.11.21	**Associative Memory**	**6**	**1,2,3,4**
	24.11.21	**Revision**	**6**	**1,2,3,4**
8	29.11.21	**Diwali Vaccation**	**--**	**--**
	30.11.21		**2-(PPT/Projector)**	**1,2,3,4**
	1.12.21	**Holiday**		
	2-Nov-22	**Data Transfer and Manipulation, Program Control**	**2-(PPT/Projector)**	**1,2,3,4**
9	6.12.21	**Virtual Memory**	**2-(PPT/Projector)**	**1,2,3,4**
	7.12.21	**Holiday**		
	8.12.21	**Memory Management Hardware**	**2-(PPT/Projector)**	**1,2,3,4**
10	13.12.21	**Input Output Organization**	**2-(PPT/Projector)**	**1,2,3,4**
	14.12.21	**Peripheral devices**	**6**	**1,2,3,4**
	15.12.21	**Input-Output Interface**	**6**	**1,2,3,4**
11	20.12.21	Asynchronous data transfer	**--**	**5**
	21.12.21	**Modes of Transfer**	**2-(PPT/Projector)**	**1,2,3,4**
	22.12.21	**Priority Interrupt**	**2-(PPT/Projector)**	**1,2,3,4**
12	27.12.21	**Direct Memory Access(DMA)**	**6**	**1,2,3,4**
	28.12.21	**Input-Output Processor(IOP)**	**2-(PPT/Projector)**	**1,2,3,4**
	29.12.21	**Design of Basic computer**	**6**	**1,2,3,4**
13	3.1.22	**Register Transfer and Microoperations**	**2-(PPT/Projector)**	**1,2,3,4**
	4.1.22	Register Transfer Language (RTL), register transfer, Bus and Memory Transfers	**9,10**	**1,2,3,4**
	5.1.22	**Logic Microoperations**	**9,10**	**1,2,3,4**
14	10.1.22	**Arithmetic Microoperations**	**2-(PPT/Projector)**	**1,2,3,4**
	11.1.22	**Shift Microoperations**	**2-(PPT/Projector)**	**1,2,3,4**
	12.1.22	**Arithmetic Logic Shift Unit**	**6**	**1,2,3,4**
15	17.1.22	**Interleaved memory**	**6**	**1,2,3,4**
	18.1.22	**MicroprogrammedControl:Control memory**	**2-(PPT/Projector)**	**1,2,3,4**
	19.1.22	**address sequencing, microprogram sequencer, Design of Control Unit, Question paper discussion**	**6**	**1,2,3,4**
16	24.1.22		**--**	**--**
	25.1.22		**--**	**--**
	26.1.22			